ABSTRACT

A two-phase non-overlapping clock generator (12) generating a sampling signal (20) utilizing a three transistor NAND gate (50). The NAND gate of the present invention eliminates one large PMOSFET (46), and has one NMOSFET (52) driven by the other phase and having its source grounded. The present invention yields substantial improvement on the jitter of the clock phases. Both rising and falling transitions are improved because of the greatly reduced self-loading of the NAND gate. Overshooting is eliminated, and the NAND gate body effect is minimized, providing enhanced jitter performance of the sampling signal and improving a signal to noise ratio (SNR). The principle of the present invention are also embodied in a NOR gate (70).